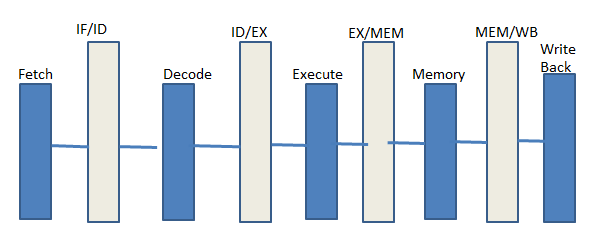
Team Members: Saroj Bardewa and Conor O'Connell

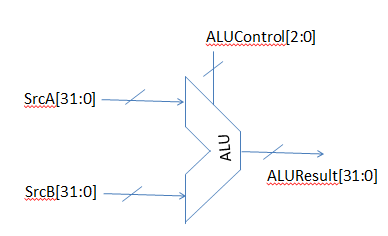
Week #5

THIS WEEK:

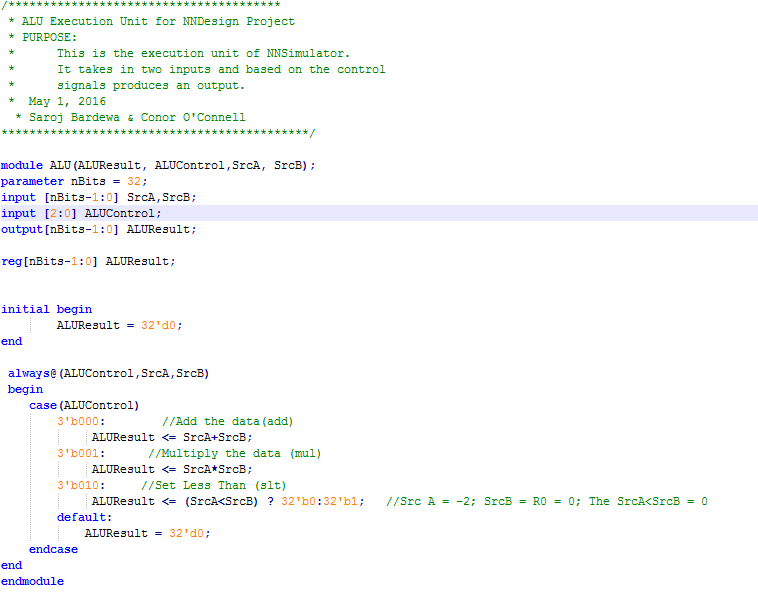
1. Researched on Pipeline processor

Our pipeline processor will consists of 5 stages- Fetch, Decode, Execution, Memory and WriteBack- with Pipeline Registers – IF/ID, ID/EX, EX/MEM, and MEM/WB. These are the standard stages in a MIPS processor. As discussed in the class, these stages are necessary, to gain higher throughput than a single-cycle processor. Our design looks like this:



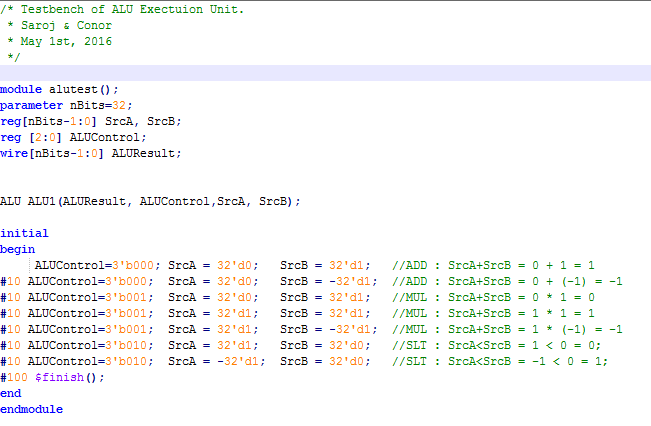
1. Designed and simulated ALU Execution Unit:

ALU is the execution unit of pipeline Neural Network system we are designing. To make the progress on pipeline design and also to review Verilog syntax, we wrote module ALU module as well as the testbench. This also allowed us to think about how we would program the execution unit to produce the desired result provided a given set up inputs.



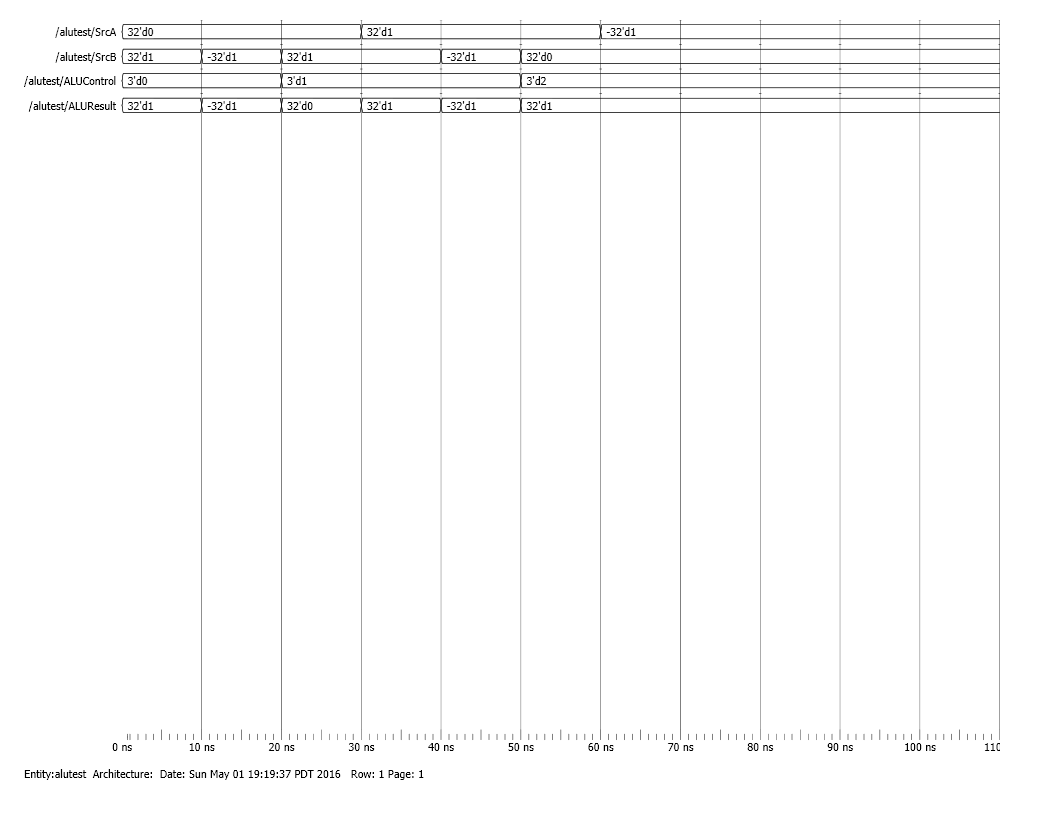
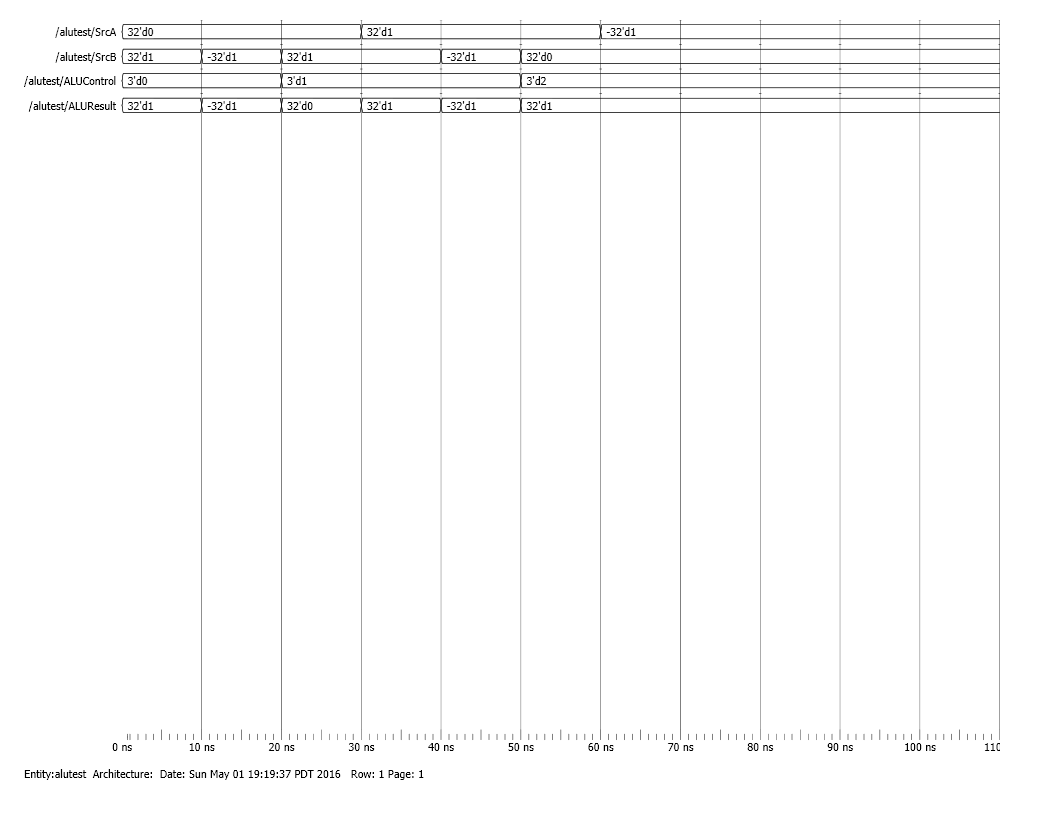
Test bench for the ALU Simulation Unit:

This is a basic test bench that tests all the functionality of the ALU.



**Result of the simulation:**

In our simulation, we had both negative and positive numbers. The result of the simulation generated exactly the results we were expecting.



1. **Conor??**

**NEXT WEEK:**

1. Work further on designing a basic pipeline NN processor.
2. Extend capability of our simulation to load in a hex textfile and save the results to a hex file
3. Complete the assembler and produce the instructions in hex format